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R E M A R K S

Careful review and examination of the subject application are noted and appreciated.

SUPPORT FOR CLAIM AMENDMENTS

Support for the amendments to the claims can be found in the drawings as originally filed, for example, on FIGS. 3, 5 and 6 and in the specification as originally filed, for example, on page 7, line 10 through page 8, line 7 and on page 25, line 1 through page 26, line 8. As such, no new matter has been added.

SUMMARY OF TELEPHONE INTERVIEW

In a telephone interview on October 6, 2003, Applicants' representative (Robert M. Miller) and Examiner Whitmore discussed claim 1 and the Uchida reference. Specifically, Applicants' representative asked that Examiner Whitmore clarify which elements in Uchida were construed to be read on by the presently pending claims. Examiner Whitmore asserted that (i) the presently claimed bond options were construed to read on elements 6 and 7 of Uchida, (ii) the presently claimed metal options were construed to read on elements 31 and 32 of Uchida, (iii) the pins for receiving the one or more voltage levels were construed to read on elements 9 and 10 of Uchida, and (iv) the claimed logical combination of (i) the one or more voltage levels on one or more inputs, (ii) a state of the

one or more bond options and (iii) a state of the one or more metal options was interpreted to correspond to a logical combination of the elements 6, 7, 31, 32 and 9 and/or 10 of Uchida (see Interview Summary, paper no. 10).

CLAIM REJECTIONS UNDER 35 U.S.C. §102

The rejection of claims 1,3-4,10, 12, 16, 17, 20-22 and 24-25 under 35 U.S.C. §102(b) as being anticipated by Uchida '304 (hereinafter Uchida) is respectfully traversed and should be withdrawn.

Uchida is directed to a semiconductor integrated circuit (Title). Uchida describes selecting an identification code for a device via bond optioning bonding pads to a GND pin during assembly (see column 3, line 58 through column 4, line 5 and column 6, lines 14-33 of Uchida). Uchida does not disclose or suggest a logic circuit configured to generate a plurality of identification codes in response to a logical combination of (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options AND (iii) a state of one or more metal options, as presently claimed. Therefore, Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over the Uchida and the rejection should be withdrawn.

Specifically, assuming, *arguendo*, that (i) elements 6 and 7 of Uchida are similar to the presently claimed bond options, (ii) GND in element 4, VCC in element 5, and elements 31 and 32 of Uchida are similar to the presently claimed metal options and (iii) elements 9 and 10 of Uchida are similar to the pins for receiving the one or more voltage levels as presently claimed (as suggested on page 2, section 4 of the Office Action and for which Applicants' representative does not necessarily agree), Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the present claims. In particular, the interpretation of elements 9 and 10 of Uchida as being similar to the presently claimed pins for receiving the one or more voltage levels is not technically correct. The elements 9 and 10 of Uchida are a shift clock input pad and a control input pad, respectively. The signal presented at the element 10 loads an ID code into a shift register formed by elements 4 and 5 of Uchida. The signal presented to the element 9 of Uchida serializes the ID code by shifting the code through the shift register formed by elements 4 and 5 of Uchida (see FIGS. 4, 8 and 9 and column 6, line 51 through column 7, line 5 of Uchida). In particular, Uchida states:

Here, when the signal for the ID setting pad 10 is turned into high level, the multiplexers 41 to 43 output the levels of A-terminals to the O-terminal. Next, when the shift clock to the shift clock pad 9 is turned into high level, high level is held in the F/F 51, low level is held in the F/F 52, high level held in the F/F 53, low level is held the F/F 54,

and then high level is output from the ID code output pad 8.

After turning the signal for the ID code setting pad 10 into low level, when shift clock for three clocks is input to the shift clock pad 9, low level, low level and high level are output in order from the ID code output pad 8.

At this time, by setting so that the ID code is output sequentially in an order from the least significant bit (LSB) to the most significant bit (MSB), the ID code "1001" can be output as the ID code for the kind C.

Similarly, for remaining kinds A, B and D, the ID codes respectively corresponding thereto can be output depending upon whether the bonding option pads 6 and 7 are bonded to the GND pins. (column 6, line 51 through column 7, line 5 of Uchida).

One skilled in the art would not consider (i) a voltage level at the pad 10 of Uchida which loads an ID code into the shift register formed by elements 4 and 5 of Uchida and (ii) a voltage level at the shift clock input pad 9 of Uchida which shifts the ID code through the shift register formed by elements 4 and 5 of Uchida to be the same as the presently claimed one or more voltage levels on one or more first inputs which are logically combined with a state of one or more bond options and a state of one or more metal options to generate a plurality of identification codes, as presently claimed.

Furthermore, Uchida does not disclose or suggest generating an ID code by **logically combining** (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options **AND** (iii) a state of one or more metal options, as

presently claimed. Specifically, the ID codes generated by the circuit of Uchida are determined **ONLY** by the bond option pads 6 and 7 and logic levels set in the diffusion process. In particular, Uchida states:

For instance, in the diffusion process, the ID code becomes "10XX[.]" In this ID code, X is "0" or "1" which is determined whether the bonding option pads 6 and 7 are bonded to the GND pins or not (column 6, lines 14-17 of Uchida, emphasis added).

With respect to generating the ID codes, Uchida further states:

When the bonding option pads 6 and 7 are both bonded to the GND pins (step S4 of FIG. 3), the IC chip becomes a kind A (step S5 of FIG. 3) and then the ID code becomes "1000".

On the other hand, when only bonding option pad 6 is bonded to the GND pin (step S6 of FIG. 3), IC chip becomes a kind B (step S7 of FIG. 3) and then the ID code becomes "1010".

Also, when only bonding option pad 7 is bonded to the GND pin (step S8 of FIG. 3), IC chip becomes a kind C (step S9 of FIG. 3) and then the ID code becomes "1001".

When the bonding option pads 6 and 7 are both not bonded to the GND pins (step S10 of FIG. 3), IC chip becomes a kind D (step S11 of FIG. 3) and then the ID code becomes "1011" (column 6, lines 18-33 of Uchida).

Since each bit of the ID codes of Uchida are directly determined by a respective bond options or diffusion, it follows that Uchida does not disclose or suggest generating an ID code by **logically combining**(i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options **AND** (iii) a state of one or more metal options, as presently claimed. The

specification provides, for example on pages 14-24, numerous examples of identification codes generated by **logically combining**(i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options **AND** (iii) a state of one or more metal options, as presently claimed.

Furthermore, the interpretation of the elements 31 and 32 of Uchida as being the same as the presently claimed metal options is not technically correct. Specifically, Uchida states:

In FIG. 2, the **bonding judgement portion 3** comprises **P-channel transistors 31 and 32**. P-channel transistors 31 and 32 are set at small current capacity so that they may **serve as pull-up resistance for the signal lines 101 and 102 from the bonding option pads 6 and 7** to the function circuit portion and the ID setting portion by connecting the gates thereof to the GND level (column 5, lines 44-50 of Uchida, emphasis added).

Rather than being separate options from the bond options, as presently claimed, the elements 31 and 32 of Uchida are integral part of the bond option capability of elements 6 and 7. In particular, elements 31 and 32 allow the signal lines 101 and 102, respectively, to become high when the bond option pads 6 and 7 are not bonded to the GND pin (see column 6, lines 46-49 of Uchida).

In contrast to Uchida, the presently claimed invention (claim 1) provides a logic circuit configured to generate a plurality of identification codes in response to a **logical combination of (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options AND (iii) a state**

of one or more metal options. Claims 16 and 20 include similar limitations. Uchida does not disclose or suggest a logic circuit configured to generate a plurality of identification codes in response to a logical combination of (i) one or more voltage levels on one or more first inputs, (ii) a state of one or more bond options AND (iii) a state of one or more metal options, as presently claimed. Therefore, Uchida does not disclose or suggest each and every element of the presently claimed invention, arranged as in the claims. As such, the presently claimed invention is fully patentable over Uchida and the rejection should be withdrawn.

Claims 2, 4-15, 17-19 and 21-25 depend, either directly or indirectly, from claims 1 or 16 which are believed to be allowable. New claim 26 depends directly from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over Uchida and the rejections should be withdrawn.

CLAIM REJECTIONS UNDER 35 U.S.C. §103

The rejection of claims 2 and 5-9 under 35 U.S.C. §103(a) as being obvious over Uchida in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990) is respectfully traversed and should be withdrawn.

The rejection of claims 11 and 13-14 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael et al. '311 (hereinafter Carmichael) is respectfully traversed and should be withdrawn.

The rejection of claim 15 and 23 under 35 U.S.C. §103(a) as being obvious over Uchida in view of Carmichael and further in view of Werger et al. '246 (hereinafter Werger) is respectfully traversed and should be withdrawn.

The rejection of claims 18-19 under 35 U.S.C. §103(a) as being obvious over Uchida in view of IBM and further in view of "IEEE Standard Test Access Port and Boundary-Scan Architecture, IEEE Std 1149.1-1990" (hereinafter IEEE Std 1149.1-1990) is respectfully traversed and should be withdrawn.

Claims 2-15, 17-19 and 21-25 depend, either directly or indirectly, from claims 1 or 16 which are believed to be allowable. New claim 26 depends from claim 1 which is believed to be allowable. As such, the presently claimed invention is fully patentable over the cited references and the rejections should be withdrawn.

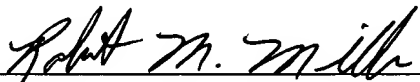
Accordingly, the present application is in condition for allowance. Early and favorable action by the Examiner is respectfully solicited.

The Examiner is respectfully invited to call the Applicants' representative should it be deemed beneficial to further advance prosecution of the application.

If any additional fees are due, please charge our office Account No. 50-0541.

Respectfully submitted,

CHRISTOPHER P. MAIORANA, P.C.



Robert M. Miller
Registration No. 42,892
24025 Greater Mack, Suite 200
St. Clair Shores, MI 48080
(586) 498-0670

Dated: December 22, 2003

Docket No.: 0325.00420